Data acquisition system of COMPASS experiment - progress and future plans

Josef Nový

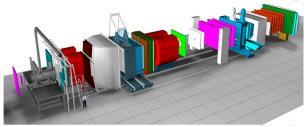
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&
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COMPASS experiment

COMPASS experiment

- fixed target experiment at SPS accelerator at CERN
- study of hadron structure and hadron spectroscopy with high intensity muon and hadron beams
- data-taking started in 2002
- trigger rate up to 50 kHz, event size 35 kB average

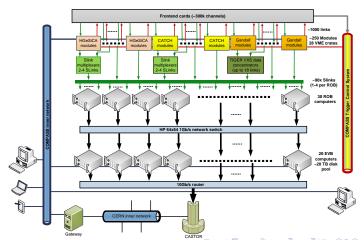


References

COMPASS experiment

Hardware/Software structure of the old DAQ

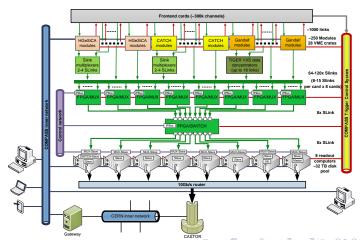
- 50 servers
- 24 older than 10 years
- Old HDD with poor performance 30 MB/s
- EB network performance 60 MB/s



Hardware/Software design of the new DAQ

Hardware/Software structure of the new DAQ

- 8 new servers 2x8 core CPU 3.6 GHz
- 32 TB disk pool
- 8 HDD in RAID 10 per server
- full events received by servers



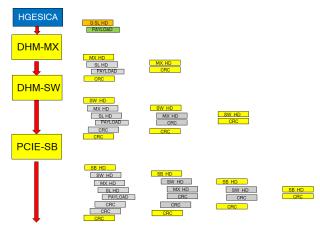
Hardware functionality

- Hardware Event builder
- HW DAQ components are synchronized by TCS
- Every data stream is checked for consistency in hardware
 - Latency, Data format, Event ID, Block size, CRC
 - OK -> data encapsulated in local Slink header
 - Tolerable error -> Preserve data and add local Slink header. with correct event number, size, CRC
 - Fatal error -> Erase data till next spill, send local Slink header and error word instead



Hardware/Software design of the new DAQ

Hardware functionality

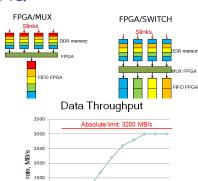


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MX/SW module for the new DAQ

- AMC module, ATCA standard
- VIRTEX6 XC6VLX130T FPGA
- 2 GB DDR3
- Module programmed as MX (15:1) or SW (8x8)







Hardware/Software design of the new DAQ

DAQ unit

- JTAG
- TCS receiver
- 1Gb Ethernet
- 16xSerial links
 - ► Slink (2Gbps)
 - Aurora(6.25 Gbps)
- 6U VME form factor module -> New DAQ fits in one 6U VME crate



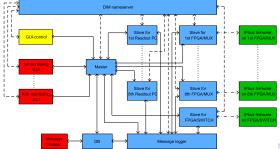
Hardware/Software design of the new DAQ

Software parts

Introduction

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- GUI runcontrol graphical user interface
- Master main control process
- SlaveReadout readout and check data
- Sharing daemon sharing events to "user" programs
- SlaveControl monitoring and control of FPGA cards

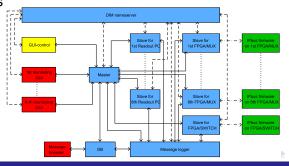


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Software parts

- database MySQL database with configuration information, system messages ...
- MessageLogger catching and logging all system messages

MessageBrowser - browsing message history and online messages



References

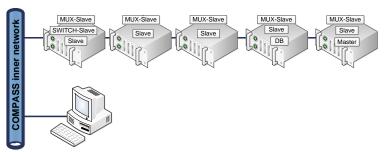
Hardware/Software design of the new DAQ

Used technologies

- ► C++, Python
- Qt framework
- MySQL
- Distributed Information Management System
- DATE (Data Acquisition and Test Environment) data format
- The IPbus suite for communication with FPGAs
- Zabbix package used for computer resources monitoring

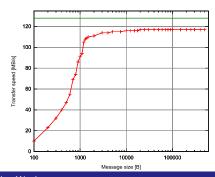
System tests phase 1 - communication tests

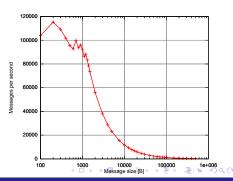
- DIM communication tests
- basic GUI design
- state machine design



DIM speed test

- new DAQ message format and random payload
- more than sufficient performance
- ▶ 1 kB messages → 92 kHz rate





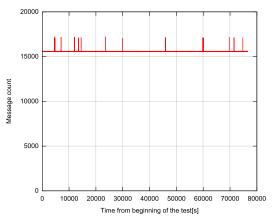
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System tests phase 1 - communication tests

DIM stability test

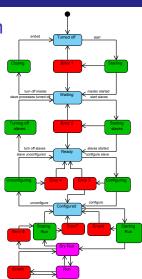
- 24-hours test
- maximum message exchange rate
- 2 DIM clients/producers
- 1 DIM server/consumer



System tests phase 1 - communication tests

State machine design

- reworked state machine design
- four types of states
- error tolerant run state

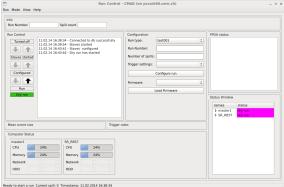


transfere states(not stable), do not accept commi error state
error state
working states, stable untile command come or end condition is

ber	name
	Turned off
	Waiting
	Ready
	Configured
	Dry Run
	Run
	Starting
	Closing
	Starting slaves
	Turning off slaves
	Configuring
	Unconfiguring
	Starting run
	Stoping Run
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Run control GUI prototype

- basic design
- basic run control
- many separate configuration windows





Ready to start a run. Current spill: 0. Timestamp: 11.02.2014 16:38:34

System tests phase 1 - communication tests

MessageBrowser, MessageLogger

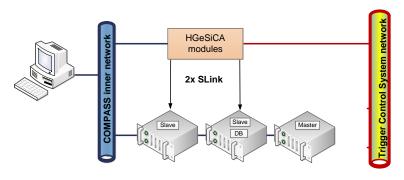
framework for logging, showing and filtering of messages





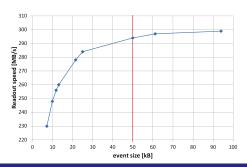
System tests phase 2 - readout tests

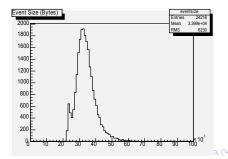
- 2xPCI-express spillbuffers
- fixed size events generated by HGeSiCa



Readout speed test

- readout speed limited by SLink transfer speed
- final DAQ with 8 spillbuffer cards speed up to 1200 MB/s
- maximum CPU usage around 40% with 4 core 2 GHz Xeon E5405

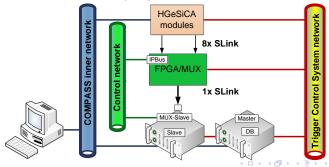




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System tests phase 3

- new hardware module
- new input data format
- new PCIe driver
- connection to "user" programs

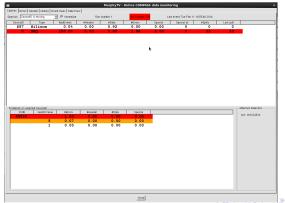


System tests phase 3 - FPGA/MUX test

System tests phase 3 - sharing daemon

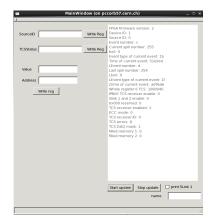
- sharing daemon prepared and tested with MurphyTv
- more extensive test to be done

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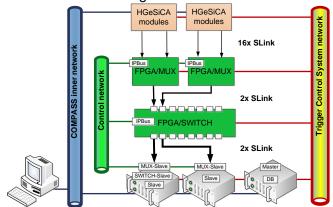
System tests phase 3 - IPbus control

- framework for communication with FPGA cards, Master, and MessageLogger
- tool to access, read, and change registers



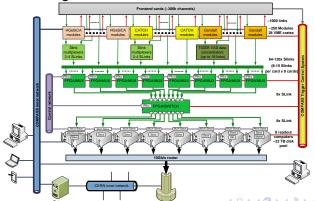
System tests phase 4

hardware event building



Full scale system test

- final software debugging
- error handling tests



- System tests phase 1 communication tests → DONE
- System tests phase 2 readout tests → DONE
- System tests phase 3 FPGA/MUX test → underway
- System tests phase 4 FPGA/SWITCH test → March-April 2014
- Full scale system test → May 2014
- Cosmic run → June-July 2014
- Pilot run → autumn 2014



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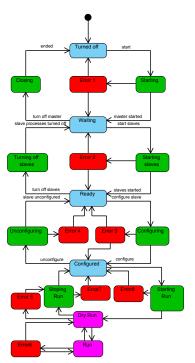
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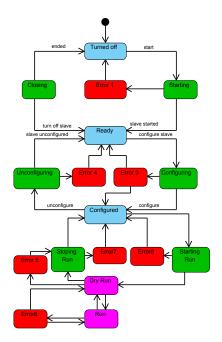
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stable state, states that do nothing just wait for next command transfers states(not stable), do not accept commi

working states, stable untile command come or end condition is reached

number	name
0	Turned off
1	Waiting
2	Ready
3	Configured
11	Dry Run
12	Run
21	Starting
22	Closing
23	Starting slaves
24	Turning off slaves
25	Configuring
26	Unconfiguring
27	Starting run
28	Stoping Run
41-48	Error 1-8



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error state